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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Paper No. 23

Application Number: 09/148,392
Filing Date: September 04, 1998
Appellant(s): BAEZ, FRANKLIN M.

THINH V. NGUYEN
For Appellant

SUPPLEMENTAL EXAMINER'S ANSWER

This is in response to the appeal brief filed September 16th, 2002 and subsequent remand from the Board of Patent Appeals and Interferences.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) Status of Claims

The statement of the status of the claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Invention

The summary of invention contained in the brief is deficient because though the general statements are correct; however the use of footnotes essentially pull into the summary large sections of the specification and goes beyond the scope of the claimed invention. Examiner summarizes the invention as follows:

Select initial design points on the parameter functions having a first sum of the constraint set, i.e. delays, and a second sum of optimizing set, i.e. power, that the first sum satisfies the design constraints, i.e. improved area usage, and selecting new design points on the parameter functions such that the second sum, i.e. power, is improved within the design constraints, i.e. improved area usage. Where the parameter function is describes the variation of one parameter as a function of another parameter. Each circuit is characterized by a parameter function. The parameter functions are the relationship between the design constraints and the optimizing parameters. In the instant case this is a graph plot between the delay and power to yield an improved area with minimized delay and power characteristics. The design constraints are a constraint set including constraint parameters; which are parameters that must be met. Where a constraint parameter is the propagation delay and the optimizing parameter is the power consumption. Alternately the propagation delay is the optimizing parameter and the power consumption is the constraint parameter.

The summation function is reproduced from the specification herein to simplify issues:

> The power and delay parameters obtained form the power-delay curves 610A, 610B, 610C, and 610D have the following values:
>
> | | | |
> |---|---|---|
> | Initial design points: | | |
> | Total delay: | .025 + 1.12 + 1.23 + 1.75 | = 4.35 nsec |
> | Total current: | 3.2 + 1.0 +10.0 + 4.0 | = 18.2 mA |
> | New design points: | | |
> | Total delay: | 0.28 + 1.05 + 1.37 + 1.65 | = 4.35 nsec |
> | Total current: | 1.6 + 1.9 + 4.0 + 6.0 | = 13.mA |
>
> Therefore, it is seen that the new design points B, D, F, H result in the same composite delay of 4.35 nsec, but with a 25.8% saving in power.

Commercial off the shelf software is used, as expressly stated throughout Applicant's specification, to generate the power (POWERMILL from EPIC) and delay (PathMill from Synopsys) data that are in turn then optimize based upon summing the parameters from each set of data such that the sizes are scaled using an area optimizing package (AMPS from EPIC). Netlists are used as in the prior art. The forgoing was taken directly from Applicant's own specification.

(6) Issues

The appellant's statement of the issues in the brief is basically correct. The only argument has been that none of the prior art references anticipate the limitations of only the independent claim 1, for example. In the spirit of compact prosecution, Examiner will only continue asserting the rejections based on the JYU et al. (967) teaching for the purposes of this Appeal. The remaining parallel rejections are just as effective as prior art, however, JYU et al. ('967) is specific to the point of using the exacting terms and commercial software as Appellant has claimed and provided for support in the Appellant's specification.

(7) Grouping of Claims

Appellant's brief includes a statement that claims 1-20 and 22-29 do stand or fall together. The claims have never been argued, beyond claim 1. During prosecution only the independent claim limitations have ever been argued and addressed by Appellant. Appellant has only recited limitations from claim 1 in the Appeal Brief as not being taught by the prior art.

(8) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) Prior Art of Record

5,880,967	JYU et al.	3-1999

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1-20, and 22-29 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by JYU ('967) et al. This rejection is set forth in prior Office Action, Paper No. 12. The remaining rejections based have been withdrawn to expedite the process. Analysis of Appellant's claims are based on JYU et al. ('967). Appellant has only argued limitations found in the independent claim 1 of rejected claims.

The following provides the Examiner's prior mapping, see paper 12, of limitations of Appellant's claims and those same teachings found in relevant sections and/or figures of JYU ('967).

Claim Rejections - 35 U.S.C. § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Claims 1-20, and 22-29 were rejected under 35 U.S.C. 102(e) as being clearly anticipated by Jyu et al.

Taking claim 1, for example, JYU ('967) teaches:

the use of integrated commercial packages of POWERMILL, col. 18, lines 28 et seq., PATHMILL col. 19, lines 26 et seq., SPICE and associative software simulators, see col. 8, lines 35-46, col. 19, lines 13-25) disclose:

A method for determining optimal values of design parameters of a subsystem (circuit with cells, Figure 28, for example) comprising a plurality of circuits, the method comprising:

creating parameter functions for a plurality of circuits in a subsystem, the subsystem having design constraints (Jyu et al: power, timing, sizing, cost), each one of the parameter functions corresponding to each one of the circuits, the corresponding circuits, the parameter functions representing a relationship among design parameters of the subsystem (cells in a circuit), the design parameters including constraint and optimizing sets, having a first sum of the constraint set and a second sum of the optimizing set such that the first sum satisfies (Figures 29, Equation 1, Equation 2, col. 10, lines 50 et seq., especially TABLE 4, Equations 4-7; further see Abstract, Figures 4A-4B, 25, 26, 6, 6A-6D, 11A-15, Figures 20-24)

selecting initial design points (Figure 6, elements 630, 632, Figure 6c, element 2902, for example) on the parameter functions having a first sum of the constraint set and a second sum of the optimizing set such that the first sum satisfies the design constraints; and (Figure 27, configuration setup, Figures 6, 6A-6D, 11A-15, Figures 20-24)

selecting new design points on the parameter functions such that the second sum is improved parameters within the design constraints (power, timing, sizing, cost) at Jyu et al.: Abstract, Figures 3, 4A-4B, circuit areas 500 and 502, flowcharts in figures 6, 6A-6E, note power/transistor parameter records 702 and 704, 706 and 708, see figure 7C, 8-10, flowcharts in figures 11A and 11B, 11C-15 (code), 16-24, region of interest in figure 25, figure 26, figures 27 and 28, col. 6, lines 6 et seq., design goals, col. 10, lines 52 et seq., POWERMILL, col. 18, lines 28 et seq., PATHMILL col. 19, lines 26 et seq.

As to claim 2, the method of claim 1, wherein the creating the parameter functions comprises:

configuring each circuit of the plurality of circuits and generating values of design parameters for each circuit according to the configuration circuit (Abstract, figures 27 and 28, col. 3, lines 40 et seq., and col. 5, lines 17 et seq.), the values providing the parameter functions are disclosed at Jyu et al.: Abstract, Figures 3, 4A-4B, circuit areas 500 and 502, flowcharts in figures 6, 6A-6E, note power/transistor parameter records 702 and 704, 706 and 708, see figure 7C, 8-10, flowcharts in figures 11A and 11B, 11C-15 (code), 16-24, region of interest in figure 25, figure 26, figures 27 and 28, col. 6, lines 6 et seq., design goals, col. 10, lines 52 et seq., POWERMILL, col. 18, lines 28 et seq., PATHMILL col. 19, lines 26 et seq.

As to claim 3, the method of claim 2, wherein, the constraint set includes constraint parameters having values selectable to meet the design constraints and the optimizing set includes optimizing parameters having values to be optimized is disclosed at Jyu et al.: Abstract, Figures 3, 4A-4B, circuit areas 500 and 502, flowcharts

in figures 6, 6A-6E, note power/transistor parameter records 702 and 704, 706 and 708, see figure 7C, 8-10, flowcharts in figures 11A and 11B, 11C-15 (code), 16-24, region of interest in figure 25, figure 26, figures 27 and 28, col. 6, lines 6 et seq., design goals, col. 10, lines 52 et seq., POWERMILL, col. 18, lines 28 et seq. , PATHMILL col. 19, lines 26 et seq.

As to claim 4, the method of claim 3, wherein optimizing comprises:

selecting values of the constraint parameters (power and delay/timing) to meet the design constraints (transistor size, cost, slack, see Figures 20-24);

determining values of the optimizing parameters (power and delay/timing) corresponding to the selected values of the constraint parameters based on the parameter functions (Figures 6, 6A -6D, 7A and 7C, and 20-24); and

iterating (ABSTRACT) the selection of values and determining of values steps until values of the optimizing parameters are within a predetermined optimal range (Figures 6A-6D, Figures 11A-25), are disclosed at Jyu et al.: Abstract, Figures 3, 4A-4B, circuit areas 500 and 502, flowcharts in figures 6, 6A-6E, note power/transistor parameter records 702 and 704, 706 and 708, see figure 7C, 8-10, flowcharts in figures 11A and 11B, 11C-15 (code), 16-24, region of interest in figure 25, figure 26, figures 27 and 28, col. 6, lines 6 et seq., design goals, col. 10, lines 52 et seq., POWERMILL, col. 18, lines 28 et seq. , PATHMILL col. 19, lines 26 et seq.

As to claim 5, the method of claim 3, wherein the constraint parameters include a delay parameter and the optimizing parameters (Figure 4, elements 408b, 414b, and 416) include a power parameter (Figure 4a, element 404b, 406b, 408b) are disclosed at

Jyu et al.: Abstract, Figures 3, 4A-4B, circuit areas 500 and 502, flowcharts in figures 6, 6A-6E, note power/transistor parameter records 702 and 704, 706 and 708, see figure 7C, 8-10, flowcharts in figures 11A and 11B, 11C-15 (code), 16-24, region of interest in figure 25, figure 26, figures 27 and 28, col. 6, lines 6 et seq., design goals, col. 10, lines 52 et seq., POWERMILL, col. 18, lines 28 et seq., PATHMILL col. 19, lines 26 et seq.

As to claim 6, the method of claim 5, wherein the design constraints include a delay constraint (figure 4a, element 412b) are disclosed at Jyu et al.: Abstract, Figures 3, 4A-4B, circuit areas 500 and 502, flowcharts in figures 6, 6A-6E, note power/transistor parameter records 702 and 704, 706 and 708, see figure 7C, 8-10, flowcharts in figures 11A and 11B, 11C-15 (code), 16-24, region of interest in figure 25, figure 26, figures 27 and 28, col. 6, lines 6 et seq., design goals, col. 10, lines 52 et seq., POWERMILL, col. 18, lines 28 et seq., PATHMILL col. 19, lines 26 et seq.

As to claim 7, the method of claim 6, wherein the step of configuring each circuit of the plurality of circuits includes sizing components in each circuit (Figure 4a, elements 416) is disclosed at Jyu et al.: Abstract, Figures 3, 4A-4B, circuit areas 500 and 502, flowcharts in figures 6, 6A-6E, note power/transistor parameter records 702 and 704, 706 and 708, see figure 7C, 8-10, flowcharts in figures 11A and 11B, 11C-15 (code), 16-24, region of interest in figure 25, figure 26, figures 27 and 28, col. 6, lines 6 et seq., design goals, col. 10, lines 52 et seq., POWERMILL, col. 18, lines 28 et seq., PATHMILL col. 19, lines 26 et seq.

As to claim 8, the method of claim 6, wherein the step of configuring each circuit of the plurality of circuits includes selecting a design technology for each circuit, the

design technology being one of static and dynamic technologies is disclosed at Jyu et al.: Abstract, Figures 3, 4A-4B, circuit areas 500 and 502, flowcharts in figures 6, 6A-6E, note power/transistor parameter records 702 and 704, 706 and 708, see figure 7C, 8-10, flowcharts in figures 11A and 11B, 11C-15 (code), 16-24, region of interest in figure 25, figure 26, figures 27 and 28, col. 6, lines 6 et seq., design goals, col. 10, lines 52 et seq., POWERMILL, col. 18, lines 28 et seq., PATHMILL col. 19, lines 26 et seq.

As to claim 9, the method of claim 7, wherein the generating values of design parameters for each circuit according to the configured circuit, the values providing the parameter functions including generating a circuit netlist (Fig. 6, elements 604-614) representing the configured circuit;

generating a timing file (figure 4a, elememnt 414b) based on the circuit netlist using a circuit critical path (Figure 8, Figure 17, elements 1142-1144); PATHMILL col. 19, lines 26 et seq.

calculating timing values by using a timing simulator (Figure 4a, element 412a); and

calculating power values by using a power estimator (Figure 4a, element 406b) is disclosed at Jyu et al.: Abstract, Figures 3, 4A-4B, circuit areas 500 and 502, flowcharts in figures 6, 6A-6E, note power/transistor parameter records 702 and 704, 706 and 708, see figure 7C, 8-10, flowcharts in figures 11A and 11B, 11C-15 (code), 16-24, region of interest in figure 25, figure 26, figures 27 and 28, col. 6, lines 6 et seq., design goals, col. 10, lines 52 et seq., POWERMILL, col. 18, lines 28 et seq.

As to claim 10, the method of claim 8, wherein selecting the new design points comprises:

selecting values of the delay parameter within the delay constraint; PATHMILL col. 19, lines 26 et seq.

determining values of the power parameter corresponding to the selected values of the delay parameter based on the parameter function; POWERMILL, col. 18, lines 28 et seq.

iterating the steps of selecting values and determining values until values of the power parameter are within a predetermined optimal range (Abstract) are disclosed at Jyu et al.: Abstract, Figures 3, 4A-4B, circuit areas 500 and 502, flowcharts in figures 6, 6A-6E, note power/transistor parameter records 702 and 704, 706 and 708, see figure 7C, 8-10, flowcharts in figures 11A and 11B, 11C-15 (code), 16-24, region of interest in figure 25, figure 26, figures 27 and 28, col. 6, lines 6 et seq., design goals, col. 10, lines 52 et seq., POWERMILL, col. 18, lines 28 et seq.

As for claims 11-20, 22-29 are rejected for the same reasoning as claims 1-10, set forth above, *supra.*.

Claims 11-20, 22-29 are equivalent machine readable medium having embodied a computer program for processing by a machine and system claims containing the same limitations and variations of limitations as recited in method claims 1-10 and taught in Jyu et al. at: Abstract, Figures 3, 4A-4B, circuit areas 500 and 502, flowcharts in figures 6, 6A-6E, note power/transistor parameter records 702 and 704, 706 and 708, see figure 7C, 8-10, flowcharts in figures 11A and 11B, 11C-15 (code), 16-24, region of

interest in figure 25, figure 26, figures 27 and 28, col. 6, lines 6 et seq., design goals, col. 10, lines 52 et seq., POWERMILL, col. 18, lines 28 et seq., PATHMILL col. 19, lines 26 et seq.

(11) Response to Argument

1) Appellant has stated what the prior art teaches in general terms however has never provided an analysis as to how the teachings of JYU et al. ('967) and the claims differ *other than to restate the claims and say that JYU et al. ('967) does not teach these limitations*. Appellant's arguments failed to comply with 37 CFR 1.111(b) because they amounted to general allegations that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references or how the claim language avoids the prior art asserted. Appellant's arguments did not comply with 37 CFR 1.111(c) because they *did not clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made*. Further, they do not show how the prior amendments avoided such references or objections, except to say that the prior art did not teach them.

The rejections were asserted under the relevant sections of 35 U.S.C 102 and are indeed provided in a clear and unambiguous manner. Further, relevant sections of each and every piece of prior art asserted under the section were identified. Examiner provided analysis and assertion of the prior art rejections.

2) Examiner would like to note that the majority of Appellant's statements in the Brief are directed to matters handled by petition not through the appeal process. Especially those raised under indent B. Examiner will not respond to these since this is believed to be the wrong venue.

3) **Summary, analysis of rejection and mapping of JYU et al. ('967) the claims**:

A summary of the JYU et al. ('967) reference is provided to help guide the Board in determining its relevance to the instant claimed invention. Looking to the specification and specifically figures 3 (resizing 300, including iteration delay/power report 332), 4A-4B (power simulation 406a, power data 408a, delay analysis 412a, timing data 414a, for initial selection 314, transistor resizer 416), flowcharts in figures 6, 6A-6D and 11A-11B, power/delay parameter records in figures 7A-7C, and graphs of delay verses power in figure 25, and power verses width in figure 26, and execution reports showing recalculations of power and delay to optimize the circuit in figures 20-24, together show the entirety of Appellant's invention, inclusive of claims 1-20, and 22-29. Power simulation uses the PowerMill product from EPIC and delay analysis is provided using PowerMill, or in the alternate PathMill also from EPIC, col. 18, lines 27 et seq. Standard netlist files and SPICE are used, col. 7, lines 63 et seq. Autosizing of the circuits is provided for at col. 13, lines 23 et seq. Netlists are used as taught in the prior art, including JYU et al. ('967) at Figure 3, item 306 (Netlist) and Figure 6, items 603-608.

The "Background of the Invention" section of JYU et al. ('967) shows how standard it is to sum the constraints to be used to iteratively optimize these parameter

functions within the design constraints as EQ 1 and EQ2 has been used in the prior art. Tables 1 - 6, and 7 are directed to analysis and improving the design using power and delay as the constraining factors with scaling up and down based on costing function responsive to changes in delay and/or power to yield an improved circuit, also see Abstract, Summary of the Invention, col. 6, lines 6 et seq., and col. 10, lines 52 et seq.

Examiner's prior rejections cite these aforementioned sections and prove related arguments and analysis, in paper 12. Appellant has used "means for" or method "steps for" construction for a number of claims that brings into the claims the means for which Appellant has recited within the specification and its equivalents, *In re Donaldson*. Specifically, the Appellants have stated that they use EPIC an off the shelf software, which is the same package as JYU et al. ('967). Both the Appellant and JYU et al.('967) use PowerMill for performing the same operations as recited in the claimed invention. Delay times can be generated using PathMill or PowerMill since either can actually provide the functionality as described in Appellant's specification.

PathMill is more specific to the static design constraints for delays as recited in claims 8, 18. Examiner has looked at this as equivalent in operation and a minor typo by Appellant during the prosecution. Further, the use of SPICE, HSPICE, SPECTRE, SPECTRE II and SPICE2 as taught in JYU et al. ('967) perform the same operations as Appellent's use of Intel SPice, ISPECE2 and provide the same functionality and produce the same resulting information, *id.*

Claims that where not constructed as "means for" have been interpreted in light of the specification, limitations from the specification are not read into the claims. See

In re Van Geuns, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). Support has been sought out in the instant case since Appellant is arguing that JYU et al. ('967) is operating in a manner differently than the claimed invention even though the same commercial software is being used for performing the same functions and yielding the same end products.

There is only one argument that revolves solely on the premise that prior art does not teach:

Select initial design points on the parameter functions having a first sum of the constraint set and a second sum of optimizing set that the first sum satisfies the design constraints and selecting new design points on the parameter functions such that the second sum is improved within the design constraints

The summation function is reproduced from the specification herein to simplify issues:

> The power and delay parameters obtained form the power-delay curves 610A, 610B, 610C, and 610D have the following values:
>
> | | | |
> |---|---|---|
> | Initial design points: | | |
> | Total delay: | .025 + 1.12 + 1.23 + 1.75 | = 4.35 nsec |
> | Total current: | 3.2 + 1.0 +10.0 + 4.0 | = 18.2 mA |
> | New design points: | | |
> | Total delay: | 0.28 + 1.05 + 1.37 + 1.65 | = 4.35 nsec |
> | Total current: | 1.6 + 1.9 + 4.0 + 6.0 | = 13.mA |
>
> Therefore, it is seen that the new design points B, D, F, H result in the same composite delay of 4.35 nsec, but with a 25.8% saving in power.

JYU et al. ('967) teaches select initial design points (init) on the parameter functions, i.e. graphs or other format of data point, having a first sum of the constraint set, i.e. delays, and a second sum of optimizing set, i.e. power, that the first sum satisfies the design constraints, i.e. improved area usage, and selecting new design points on the parameter functions such that the second sum, i.e. power, is improved within the design constraints, i.e. improved area usage. [see figures 3 (resizing 300, including iteration delay/power report 332), 4A-4B (power simulation 406a, power data 408a, delay analysis 412a, timing data 414a, for initial selection 314, transistor resizer 416), flowcharts in figures 6, 6A-6D and 11A-11B, power/delay parameter records in figures 7A-7C, and graphs of delay verses power in figure 25, and power verses width in figure 26, and execution reports showing recalculations of power and delay to optimize the circuit in figures 20-24, together show the entirety of Appellant's invention. Power simulation uses the PowerMill product from EPIC and delay analysis is provided using PowerMill, or in the alternate PathMill also from EPIC, col. 18, lines 27 et seq. Standard netlist files and SPICE are used, col. 7, lines 63 et seq. Autosizing or optimizing of the circuits is provided for at col. 13, lines 23 et seq.]

where the summation function is reproduced from the specification herein to simplify issues:

> The power and delay parameters obtained form the power-delay curves 610A, 610B, 610C, and 610D have the following values:
>
> | | | |
> |---|---|---|
> | Initial design points: | | |
> | Total delay: | .025 + 1.12 + 1.23 + 1.75 | = 4.35 nsec |
> | Total current: | 3.2 + 1.0 +10.0 + 4.0 | = 18.2 mA |
> | New design points: | | |
> | Total delay: | 0.28 + 1.05 + 1.37 + 1.65 | = 4.35 nsec |

Total current: 1.6 + 1.9 + 4.0 + 6.0 = 13.mA

Therefore, it is seen that the new design points B, D, F, H result in the same composite delay of 4.35 nsec, but with a 25.8% saving in power.

In JYU et al. ('967) at the "Background of the Invention" section disclose standard summing of constraints (power and delay) to be used to iteratively optimize these parameter functions within the design constraints as EQ 1 and EQ2 have been used in the prior art. Note that figures 20-24 are directed to iterative designs with % changes in power, delay, width and cost. also see Abstract, Summary of the Invention, col. 6, lines 6 et seq., and col. 10, lines 52 et seq. and Tables 1 - 6, and 7 which are all directed to analysis and improving the design using power and delay as the constraining factors with scaling up and down based on costing function responsive to changes in delay and/or power to yield an improved circuit.

Appellant is using well known technologies and methodologies to affect designs within a circuit framework. The engineer, one of ordinary skill level for example the undergraduate in electrical engineering, using a simulation-modeler-optimizer will always have design constraints and sum a first constraint set (first sample base) and a second sum of the optimizing set (next sample base) and continue to optimized the design with constrained parameters that meet the design model. This includes setting two parameters sets against one another to yield operational constraints that are used to optimize the layout.

In fact, based on the teaching of Appellant's own specification the products are commercially available as COTS products performing their intended use. This is merely using the well known tool of the trade for its specific purpose. The courts have held that

"A reference anticipates a claim if it discloses the claimed invention such that a skilled artisan could take its teachings in combination with his own knowledge of the particular art and be in possession of the invention." *In re Graves, 36 USPQ2d 1697 (Fed. Cir. 1995); In re Sase, 207 USPQ 107 (CCPA 1980); In re Samour, 197 USPQ 1 (CCPA 1978).* One of ordinary skill level that resizes transistors uses the two primary physical characteristics of the device which are power consumption and delays based upon signal pathway characteristics. This is expressly taught in JYU et al. and is common and well established knowledge to those skilled in the arts.

Appellant's components and their operations are taught within JYU et al. which uses the exact same or equivalent methodologies or devices which are identical in operation and provide there inherent operations (power to determine power data, delay to determine timing data) that have an inevitable presence and are well known in the art. *In re Bond, 15 USPQ2d 1566 (Fed. Cir. 1990), In re Robertson, 49 USPQ2d 1949 (Fed. Cir. 1999)* Therefore, JYU et al., clearly anticipates Applicant's claimed invention. Moreover, Applicants' have not disclosed or claimed any limitations that are patentably distinguishable over JYU et al. The prior art teaching of JYU et al. *explicitly* uses the *same software and integration* of data *to yield the same end system that Appellant has claimed inventive.* The well established commercial products and there well established integration and interrelations are used, were designed and made to operated to provide engineering optimizations between these well established and known parameters for circuit designs. Appellant is currently claiming a system that uses timing or propagation delays and power parameters to optimize transistor sizing. The relationships between

these two parameters and the sizing of a circuit are well known in the art, as taught by JYU et al. The use of a computer system to optimize the layout and sizing of the circuit based on these parameters is just as old in the art, see Background of the Invention section of JYU et al.

For the above reasons, it is believed that the rejections should be sustained.

WILLIAM THOMSON
SUPERVISORY PATENT EXAMINER

Respectfully submitted,

William D. Thomson
SPE TC 2100
March 15, 2006

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